What is claimed is:

1. An encryption device for performing encryption of plain text blocks using data encryption standard algorithm, wherein the encryption device includes an initial permutation unit, a data encryption unit having n-stage (n is an even number equal to or larger than four) pipeline structure using a first clock and a second clock and an inverse initial permutation unit, the encryption device comprising:

a multiplexer for selecting one of a half of n 48-bit inputs;

8 S-Boxes, each for receiving 6-bit address among the selected 48-bit and outputting 4-bit data;

a demultiplexer for distributing 4-bit data from each of the S-Boxes to the half of n outputs; and

a controller for control the multiplexer and the demultiplexer with a third clock and a fourth clock,

wherein the third and the fourth clock are faster than the first and the second clocks by n/2 times.

2. The device as recited in claim 1, wherein the third clock is an inverse signal of the fourth clock.

3. The device as recited in claim 2, wherein the multiplexer and the demultiplexer perform time division between the half of n input paths and between the half of n output paths, respectively, to thereby avoid data collision.

4. An encryption device for performing encryption of plain text blocks using data encryption standard algorithm, wherein the encryption device includes an initial permutation unit, a data encryption unit having 8-stage pipeline structure using a first clock and a second clock and an inverse initial permutation unit, the encryption device comprising:

a first multiplexer for selecting one of a first and a second 48-bit inputs;

a first S-Box unit having 8 S-Boxes, each S-Box for receiving 6-bit address among selected 48-bit from the first multiplexer and outputting 4-bit data;

a first demultiplexer for distributing 4-bit data from each of the S-Boxes to one of a first and a second outputs;

a first controller for controlling the first multiplexer and the first demultiplexer with a third clock and a fourth clock;

a second multiplexer for selecting one of a third and fourth 48-bit inputs;

a second S-Box unit having 8 S-Boxes, each S-Box for receiving 6-bit address among selected 48-bit from the second multiplexer and outputting 4-bit data;

a second demultiplexer for distributing 4-bit data from each of the S-Boxes to one of a third and a fourth outputs; and

a second controller for controlling the second multiplexer and the second demultiplexer with the third clock and the fourth clock,

wherein the third and the fourth clocks are faster than the first and the second clocks by two times.

5. The device as recited in claim 4, wherein the third clock is an inverse signal of the fourth clock.

6. The device as recited in claim 5, wherein the first multiplexer and the first demultiplexer perform time division between two input paths and between two output paths, respectively, to thereby avoid data collision.

7. The device as recited in claim 6, wherein the second multiplexer and the second demultiplexer perform time division between two input paths and between two output paths, respectively, to thereby avoid data collision.